IFW

Docket No.: U1927.0014
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yuji Ando et al.

Application No.: 10/518,602

Confirmation No.: 5070

Filed: December 17, 2004

Art Unit: 2815

For: SEMICONDUCTOR DEVICE HAVING SCHOTTKY JUNCTION ELECTRODE

Examiner: M. C. Landau

SUBMISSION OF VERIFIED TRANSLATION OF PRIORITY DOCUMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Amendment dated August 25, 2005, and in support thereof, Applicants submit herewith a verified translation of Japanese Patent Appln. No. 2002-175243, filed June 17, 2002. The filing of this translation removes Taniguchi (US 2003/0107065) as a reference against the claims.

Dated: August 30, 2005

Respectfully submitted,

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DOCSNY.161776.1

VERIFICATION OF THE TRANSLATION

I, the below-named Chartered Patent Attorney of Tokyo Japan having an office at an address stated below, hereby declare that:

I am knowledgeable in the English and Japanese languages, and I believe that the attached English translation of the Japanese Patent Application No. 2002-175243 filed on June 17, 2002 is a true and complete translation of said application.

I also hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: August 29, 2005

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[Kind of Document] Application for patent
[Reference Number] 33409891
[Date of Submission] June 17, 2002
[Address] The Commissioner of the Patent Office
[IPC] H01L 21/80
H01L 21/80

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[Account No.] 003399

[Official Fee Paid] 21,000 yen

[List of Attached Document]

[Kind of Document] Specification 1 copy

[Kind of Document] Drawings 1 copy

[Kind of Document] Abstract 1 copy

[Number of General Power of Attorney] 9002137

[Proof] Necessary

Abstract

[Object]

It is an object of the present invention to provide a high power performance, high reliability GaN semiconductor device by improving thermal stability of a Schottky junction electrode.

[Methods for achieving the object]

A GaN semiconductor device with improved heat resistance of the Schottky junction electrode and excellent power performance and reliability is provided. In the semiconductor device having a Schottky gate electrode 17 contacting with an AlGaN electron supplying layer 14, the gate electrode 17 has a laminated structure comprising a first metal layer 171 formed with any one of Ni, Pt and Pd, a second metal layer 172 formed with any one of Mo, Pt, W, Ti, Ta, MoSi, PtSi, WSi, TiSi, TaSi, MoN, WN, TiN and TaN, and a third metal layer formed with any one of Au, Cu, Al and Pt. Since the second metal layer is a material having a high melting point, it works as a barrier to the interdiffusion between the first metal layer and the third metal layer, and the deterioration of the gate characteristics caused by high temperature operation is suppressed. Since the first metal layer contacting with the AlGaN electron supplying layer 14 has a large work function, the Schottky barrier is high, and a superior Schottky contact is obtained.

[Selected figure] Figure 1

Specification

SEMICONDUCTOR DEVICE

[Claim 1] A semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer,

wherein said Schottky junction electrode comprises a laminated structure in which a first metal layer is formed on said semiconductor layer, a second metal layer is formed on the first metal layer, and a third metal layer is formed on the second metal layer,

wherein said first metal layer comprises any material selected from a group of Ni, Pt, Pd, Ni_zSi_{1-z}, Pt_zSi_{1-z}, Pd_zSi_{1-z}, Ni_zN_{1-z}, and Pd_zN_{1-z} (where, $0<z<1$);

wherein said second metal layer comprises any material selected from a group of Mo, Pt, W, Ti, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$); and

wherein said third metal layer comprises any material selected from a group of Au, Cu, Al, and Pt.

[Claim 2] A semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer,

wherein said Schottky junction electrode comprises a laminated structure in which a first metal layer is formed on said semiconductor layer and a second metal layer is formed on the first metal layer,

wherein said first metal layer comprises any material selected from a group of Ni_ySi_{1-y}, Pt_ySi_{1-y}, Pd_ySi_{1-y}, Ni_yN_{1-y}, and Pd_yN_{1-y} (where, $0<y<1$); and

wherein said second metal layer comprises any material selected from a group of Au, Cu, Al and Pt.

[Claim 3] A semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main

component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer,

wherein said Schottky junction electrode comprises a laminated structure in which a first metal layer is formed on said semiconductor layer, a second metal layer is formed on the first metal layer, and a third metal layer is formed on the second metal layer,

wherein said first metal layer comprises any material selected from a group of $Ni_{z1}Si_{1-z1}$ (where, $0.4 \leqq z1 \leqq 0.75$), $Pt_{z2}Si_{1-z2}$ (where, $0.5 \leqq z2 \leqq 0.75$), $Pd_{z3}Si_{1-z3}$ (where, $0.5 \leqq z3 \leqq 0.85$), $Ni_{z4}N_{1-z4}$ (where, $0.5 \leqq z4 \leqq 0.85$), and $Pd_{z5}N_{1-z5}$ (where, $0.5 \leqq z5 \leqq 0.85$);

wherein said second metal layer comprises any material selected from a group of Mo, Pt, W, Ti, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$); and

wherein said third metal layer comprises any material selected from a group of Au, Cu, Al, and Pt.

[Claim 4] A semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer,

wherein said Schottky junction electrode comprises a laminated structure in which a first metal layer is formed on said semiconductor layer and a second metal layer is formed on the first metal layer,

wherein said first metal layer comprises any material selected from a group of $Ni_{y1}Si_{1-y1}$ (where, $0.4 \leqq y1 \leqq 0.75$), $Pt_{y2}Si_{1-y2}$ (where, $0.5 \leqq y2 \leqq 70.5$), $Pd_{y3}Si_{1-y3}$ (where, $0.5 \leqq y3 \leqq 0.85$), $Ni_{y4}N_{1-y4}$ (where, $0.5 \leqq y4 \leqq 0.85$), and $Pd_{y5}N_{1-y5}$ (where, $0.5 \leqq y5 \leqq 0.85$); and

wherein said second metal layer comprises any material selected from a group of Au, Cu, Al and Pt.

[Claim 5] A semiconductor device according to any one of claims 1 to 4, wherein said semiconductor layer is formed on a plurality of compound semiconductor layers formed on any one of a sapphire substrate, a SiC substrate, and a GaN substrate.

[Claim 6] A semiconductor device according to any one of claims 1 to 5, wherein said semiconductor layer is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

[Claim 7] A semiconductor device according to any one of claims 1 to 5, wherein said semiconductor layer is a AlGaN electron supplying layer formed on any one of a GaN channel layer and InGaN channel layer.

[Claim 8] A semiconductor device according to any one of claim 1 to 5, wherein said semiconductor layer is any one of a GaN channel layer and InGaN channel layer formed on an AlGaN electron supplying layer.

[Claim 9] A semiconductor device according to any one of claims 1 to 5, wherein said semiconductor layer is an n-type GaN channel layer.

[Detailed Explanation of the Invention]

[Field of Industrial Application]

The present invention relates to a high power semiconductor device used in a microwave band including GaN as a principal material. Particularly, the present invention relates to a Schottky junction electrode used for a semiconductor device superior in heat resistance and power.

Background of the Art

Fig. 8 is a cross sectional view of a conventional semiconductor device of this kind. The semiconductor device has been reported, for example, in IEEE Trans. Microwave Theory Tech. (Vol. No. 46, No. 6, Page 756, 1998) authored by U. K. Mishra et al.

As shown in Fig. 8, the semiconductor device is a heterojunction field-effect transistor which has a semiconductor layer formed on a sapphire substrate. A buffer layer 62 comprising aluminum nitride (AlN), a gallium nitride (GaN) channel layer 63, and an aluminum gallium nitride (AlGaN) electron supplying layer 64 are sequentially formed on the sapphire substrate 61, and the laminated body of the semiconductor layers is thus configured on the sapphire substrate 61.

In addition, a source electrode 6S and a drain electrode 6D are formed in contact with the AlGaN electron supplying layer 64, and these source electrode 6S and drain electrode 6D are in ohmic contact with the AlGaN electron supplying layer 64. Furthermore, a gate electrode 67 is formed in contact with the AlGaN electron supplying layer 64, and this gate electrode 67 is in Schottky contact with the AlGaN

electron supplying layer 64. The gate electrode 67, in this case, is a laminated structure comprising a Ni layer 671and an Au layer 672.

[Issues to be solved by the Invention]

In the Schottky interface of GaN semiconductors comprising GaN, AlGaN or the like, since an influence of pinning of the Fermi level is small, the barrier height (ΦB) is determined by the difference between the work function (Wm) of a metal and the electron affinity (χs) of a semiconductor.

$$\Phi B = Wm - \chi s \quad (1)$$

Therefore, the Schottky junction electrode 67 of a semiconductor device using a prior art has been in contact with the AlGaN layer 64, and had a metal layer 671 composed of, for example, Ni, Pt, Pd or the like, which have a large work function. In addition, an Au layer 672 is formed on the metal layer 671 for reducing the resistance of the electrode.

If Ni, Pt and Pd are used to form the Schottky junction electrode 67, a high Schottky barrier is obtained. However, there exists a thermal unstability, for example, a low transition point of Ni, which is approximately 353°C. In a semiconductor device using GaN as a principal material, it is possible to operate at high power density (1 to 10W/mm) because high current density (up to 1A/mm) and high breakdown voltage (up to 100V) can be obtained with the device. Under such operating conditions, since the temperature in the vicinity of the gate electrode rises to over 400°C by self-heating, thermal diffusion and alloying reaction of Ni, Pt and Pd with Au which constitutes the metal layer 672 has been significant.

In order to confirm these phenomena, a heat treatment was performed (for 15 minutes at 500 ℃) on the conventional semiconductor device shown in Fig 8. Fig. 9 is a diagram showing the gate reverse current – voltage characteristics measured before and after the heat treatment. In Fig. 9, the vertical axis indicates the gate current (A/mm) and the horizontal axis indicates the gate – drain voltage (V). According to Fig. 9, it was confirmed that the gate reserve current was increased by about one order through the heat treatment on the conventional semiconductor.

Morcover, depth profiles of the constituent elements before and after the heat treatment of the conventional semiconductor device were examined by using Auger spectroscopy. Fig. 10 is a diagram showing the Auger profile before the heat treatment. Fig. 11 is a diagram showing the Auger profile after the heat treatment. In Fig. 10 and Fig. 11, the vertical axis indicates the Auger strength (a. u.) and the horizontal axis indicates the sputtering time (minute). It has been confirmed that the interdiffusion of

Ni and Au was generated by the heat treatment at 500°C on the conventional semiconductor device. Therefore, the increase of the gate reverse current by the heat treatment is considered to be due to deterioration of the Schottky barrier at the interface with the AlGaN electron supplying layer 64 by promotion of alloying of Ni and Au, and a work function of NiAu alloy is smaller than that of Ni. In addition, there was a problem that, at high temperatures, thermal diffusion of Ni configuring the Schottky junction electrode 671 into the AlGaN electron supplying layer 64 takes place, thereby forming a deep level, and resulting in destabilizing of the device characteristics.

The present invention has been developed in light of the afore-mentioned problems of the prior art. Therefore, the purpose of the present invention is to improve the heat resistance of the Schottky junction electrode and to provide a semiconductor device using GaN as a principal material, which has an excellent power performance and reliability.

[Method for Solving the Problems]

To solve the above problems, the present invention provides a semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer, wherein said Schottky junction metal layer comprises a laminated structure in which a first metal layer is formed on said semiconductor layer, a second metal layer is formed on the first metal layer, and a third metal layer is formed on the second metal layer, wherein said first metal layer comprises any material selected from a group of Ni, Pt, Pd, Ni_zSi_{1-z}, Pt_zSi_{1-z}, Pd_zSi_{1-z}, Ni_zN_{1-z}, and Pd_zN_{1-z} (where, $0<z<1$); wherein said second metal layer comprises any material selected from a group of Mo, Pt, W, Ti, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$); and wherein said third metal layer comprises any material selected from a group of Au, Cu, Al, and Pt.

In addition, the present invention provides a semiconductor device having a semiconductor layer configured with a compound semiconductor containing Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of Group III-elements and N as a main component of Group V-elements, and a Schottky junction electrode contacting with the semiconductor layer, wherein said Schottky junction metal layer comprises a laminated structure in which a first metal layer is formed on said semiconductor layer and a second metal layer is formed on the first metal layer, wherein said first metal layer comprises any material selected from a group of Ni_ySi_{1-y}, Pt_ySi_{1-y}, Pd_ySi_{1-y}, Ni_yN_{1-y}, and

Pd_yN_{1-y} (where, $0<y<1$); and wherein said second metal layer comprises any material selected from a group of Au, Cu, Al and Pt.

It is favorable that the semiconductor layer is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

[Effectiveness]

In the stacked layer structure comprising the first metal layer to the third metal layer, the second metal layer suppress interdiffusion between the first metal layer and the third metal layer, thereby resulting in improvement of the reliability. In addition, since a work function of the first metal is large, the Schottky barrier becomes high, thereby resulting in a semiconductor device having a good Schottky contact. Also, in the stacked layer structure comprising the first metal layer and the second metal layer, a thermal diffusion of the first metal layer into GaN semiconductor is suppressed, thereby resulting in improvement of the reliability. Accordingly, the present invention largely contributes to high temperature performance and high output power of the semiconductor device.

[Embodiments of the Invention]

Examples of embodiments of the present invention will be explained by referring to figures.

(First Embodiment)

A first embodiment according to the present invention will be explained by referring to Fig. 1, Fig. 2, and Fig. 3.

Fig. 1 is a figure showing a cross sectional structure of an AlGaN/GaN heterojunction field-effect transistor (Hetero-Junction Field Effect Transistor: HJFET) in the first embodiment according to the present invention. The transistor is formed on a sapphire substrate 11. In Fig. 1, an undoped AlN buffer layer 12 is formed on the sapphire substrate 11, next, an undoped GaN channel layer 13 is formed on the undoped AlN buffer layer 12, and an undoped AlGaN electron supplying layer 14 is formed on the undoped GaN channel layer 13, sequentially. Furthermore, a source electrode 6S and a drain electrode 6D are formed in contact with the AlGaN electron supplying layer 14. The source electrode 6s and the drain electrode 6D are in ohmic contact with the AlGaN electron supplying layer 14. Furthermore, a gate electrode 17 composed of a three-layers structure comprising a Ni layer 171 contacting with the AlGaN electron supplying layer 14, a Mo layer 172 contacting with the Ni layer 171, and an Au layer 173 contacting with the Mo layer, is formed. The gate electrode is in Schottky contact

with the AlGaN electron supplying layer 14. In addition, accompanying the piezo polarization effect and spontaneous polarization effect caused by the difference in lattice constant between GaN and AlGaN, a two-dimensional electron gas is generated within the GaN channel layer 13 in the vicinity of the interface with the AlGaN electron supplying layer 14. The HJFET operates as a transistor by modulating the concentration of the two-dimensional electron gas with a potential of the gate electrode 17.

A semiconductor device according to this embodiment is fabricated in the following manner. An undoped AlN layer 12 with a film thickness of 20 nm, an undoped GaN layer 13 with a film thickness of 2 μm, and an undoped $Al_{0.3}Ga_{0.7}N$ electron supplying layer 14 with a film thickness of 30 nm, are sequentially grown on the sapphire substrate 11 which has (0001) surface orientation by, for example, a Molecular Beam Epitaxy (MBE) method.

Here, although the lattice constants of AlGaN and GaN are different, the film thickness of 30 nm of the undoped $Al_{0.3}Ga_{0.7}N$ electron supplying layer 14 is less than the critical film thickness for generating dislocations.

Next, the source electrode 6S and the drain electrode 6D are each formed on the AlGaN electron supplying layer 14, for example, by evaporating metals such as Ti/Al and alloying the metals to form ornic contact. .Finally, metal layers are sequentially formed on the AlGaN electron supplying layer 14 in the sequence and with the thicknesses described below, for example, by evaporation/lift-off method to form the gate electrode 17 with a Schottky contact . A first Ni metal layer 171 having a thickness of 15 nm is formed on the AlGaN electron supplying layer 14; next, a second Mo metal layer 172 having a thickness of 15 nm is formed on the first metal layer 171; and a third Au metal layer 173 having a thickness of 200 nm is formed on the second metal layer 172.

Through the above processes, the semiconductor device shown in Fig. 1 is fabricated.

The specific point of this embodiment lies in the fact that the Schottky gate electrode 17 is composed of a three-layer structure comprising the first Ni layer 171, the second Mo layer 172, and the third Au layer 173. Since Mo has a high melting point of approximately 2,630°C, it works as a barrier for the interdiffusion of Ni and Au. Therefore, the gate leak current is suppressed even at high temperatures, and as a result, the reliability of the device has been improved. In addition, since the first metal Ni contacting with the AlGaN electron supplying layer 14 has a large work function of

approximately 4.6 eV, the Schottky barrier is high, and an excellent Schottky contact can be obtained.

A heat treatment (15 minutes at 500°C) was performed on the semiconductor device. The gate reverse current – voltage characteristics before and after the heat treatment is shown in Fig. 2. In Fig. 2, the vertical axis indicates the gate current (A/mm) and the horizontal axis indicates the gate-drain voltage (V). As shown in Fig. 2, almost no change was observed in the gate reverse current before and after the heat treatment, resulting in confirmation of the effect of the improved heat resistance by inserting the Mo layer.

Fig. 3 is a characteristic diagram showing a gate width dependency of the saturated output density of the semiconductor device in this embodiment, compared with that of a conventional semiconductor device. In Fig. 3, the vertical axis indicates the saturated power (W/mm) and the horizontal axis indicates the gate width of the semiconductor device (mm). In the figure, measurement results of the conventional semiconductor device are also shown. Regarding the conventional technology, in a large device having a gate width of more than 32 mm, it was observed that the saturated output density dropped significantly due to self-heating. On the other hand, a decrease of output power density in this embodiment of the present invention was small. Then, the improvement of power by the improved heat resistance of the gate electrode was also confirmed.

In this embodiment, even though Mo was used for forming the second metal layer with a Mo layer 172, the foregoing effect can be obtained even if the Mo layer is replaced with, for example, other refractory metal layer. For example, the second metal layer (172) may be replaced with any one of a Pt layer, a W layer, a Ti layer, and a Ta layer.

The same effect can be obtained even if the afore-mentioned metal elements are replaced with intermetallic compounds such as metal silicates or metal nitrides which are thermally stable and have a high melting point. For example, the second metal layer 172 can be replaced with any one of a Mo_xSi_{1-x} layer, a Pt_xSi_{1-x} layer, a W_xSi_{1-x} layer, a Ti_xSi_{1-x} layer, a Ta_xSi_{1-x} layer, a Mo_xN_{1-x} layer, a W_xN_{1-x}, a Ti_xN_{1-x} layer, and a Ta_xN_{1-x} layer (where, $0<x<1$ for the all in the above).

In this embodiment according to the present invention, although the first metal layer was configured with a Ni layer 171, the foregoing effect can be obtained even if the Ni layer is replaced with, for example, other metal element having a large working function. For example, the first metal layer 171 may be replaced with a Pt layer and a Pd layer.

In addition, in this embodiment, although the third metal layer was formed with an Au layer, the foregoing effect can be obtained even if the Au layer is replaced with, for example, other metal layer having a low resistivity. For example, the third metal layer (173) may be replaced with a Cu layer, an Al layer, and a Pt layer.

(Second Embodiment)

Next, a second embodiment according to the present invention will be described by referring to Fig. 4.

Fig. 4 is a figure showing a cross sectional structure of an AlGaN/GaN HJFET in the second embodiment according to the present invention. The HJFET is configured on a semiconductor layer formed on a sapphire substrate 21. On the substrate 21, an undoped AlN buffer layer 22 (20 nm) is formed, an undoped GaN channel layer 23 (film thickness: 2 μm) is formed on the AlN buffer layer 22, and an AlGaN electron supplying layer 24 of undoped $Al_{0.3}Ga_{0.7}N$ (film thickness: 30 nm) is formed on the GaN channel layer 23, sequentially.

A source electrode 6S and a drain electrode 6D are formed in contact with the upper surface of the AlGaN electron supplying layer 24. The source electrode 6S and the drain electrode 6D are in ohmic contact with the AlGaN electron supplying layer 24. Furthermore, a gate electrode 27, which has a laminated structure comprising a NiSi layer 271 (15 nm) as a first metal layer composed of $Ni_{0.7}Si_{0.3}$ which contact with the AlGaN electron supplying layer 24 and an Au layer 272 (200 nm) as a second metal layer, is formed. The gate electrode is a Schottky contact with the AlGaN electron supplying layer 24. Accompanying the piezo polarization effect and the spontaneous polarization effect caused by the difference of lattice constant between GaN and AlGaN, a two-dimensional electron gas is generated within the GaN channel layer 23 in the vicinity of the interface with AlGaN electron supplying layer 24. The HJFET operates as a transistor by modulating the concentration of the two-dimensional electron gas with the potential of the gate electrode 27.

The specific feature of this embodiment lies in the fact that the gate electrode 27 has a laminated structure comprising a $Ni_{0.7}Si_{0.3}$ first metal layer 271 and an Au second metal layer 272. Since the bonding force between Ni and Si in Ni_ySi_{1-y} (where, $0<y<1$) is strong, Ni_ySi_{1-y} is more stable than simple Ni at high temperature. Preferably, y is $0.4 \leqq y \leqq 0.75$. Especially, if $0.65 \leqq y \leqq 0.75$, the melting point is extremely high, approximately at 1200°C or higher, and, in addition, preferably, the resistivity increase is small compared with Ni. With the above reason, thermal diffusion of a metal of the

first metal layer 271 into the AlGaN electron supplying layer 24 is suppressed even at high temperature. As a result, reliability of the device is improved.

In this embodiment according to the present invention, although the first metal layer was configured with a NiSi layer 271, the foregoing effect can be obtained even if the first metal layer (271) is replaced with, for example, other intermetallic compounds of metal silicates or metal nitrides which have a large work function and a high thermal stability, for example, PtSi, PdSi, NiN, and PdN. It is favorable to form the first metal layer (271) with any one of Pt_ySi_{1-y} (where, $0.5 \leqq y \leqq 0.75$), Pd_ySi_{1-y} (where, $0.5 \leqq y \leqq 0.85$), Ni_yN_{1-y} (where, $0.5 \leqq y \leqq 0.85$), and Pd_yN_{1-y} (where, $0.5 \leqq y \leqq 0.85$). Furthermore, in this embodiment according to the present invention, although the second metal layer was configured with an Au layer 272, the foregoing effect can be obtained even if the Au layer is replaced with, for example, other metal layer which has a low resistivity. For example, the second metal layer (272) may be replaced with any one of a Cu layer, an Al layer, and a Pt layer.

(Third Embodiment)

Next, a third embodiment according to the present invention will be described by referring to Fig. 5.

Fig. 5 is a figure showing a cross sectional structure of an AlGaN/GaN HJFET in the third embodiment according to the present invention. The HJFET is configured with a semiconductor layer formed on a SiC substrate 31. On the SiC substrate 31, an undoped AlN buffer layer 32 is formed, an undoped GaN buffer layer 33 (film thickness: 2 μm) is formed on the undoped AlN buffer layer 32, an InGaN channel layer 34 composed of an undoped $In_{0.1}Ga_{0.9}N$ (film thickness:15 nm) is formed on the undoped GaN buffer layer 33, and an AlGaN electron supplying layer 35 composed of an undoped $Al_{0.2}Ga_{0.8}N$ (film thickness: 40 nm) is formed on the InGaN channel layer 34, sequentially.

A source electrode 6S and a drain electrode 6D are formed in ormic contact on an upper surface of the AlGaN electron supplying layer 35. Furthermore, a gate electrode 37 having a laminated structure comprising a NiSi layer 371 as a first metal layer composed of $Ni_{0.7}Si_{0.3}$ which contact with the AlGaN electron supplying layer 35, a Mo layer 372 as a second metal layer, and an Au layer 373 as a third metal layer, is formed in Schottky contact. Accompanying the piezo polarization effect and the spontaneous polarization effect caused by the difference of lattice constant between InGaN and AlGaN, a two-dimensional electron gas is generated within the InGaN channel layer 34 in the vicinity of the interface with the AlGaN layer 35. The HJFET operates as a

transistor by modulating the concentration of the two-dimensional electron gas with a potential of the gate electrode 37.

The specific feature of this embodiment lies in the fact that the gate electrode 37 has a laminated structure comprising a NiSi layer 371, a Mo layer 372, and an Au layer 272. Since Mo has a high melting point, approximately at 2650°C, it works as a barrier for the interdiffusion of Ni and Au. As a result, the gate leakage is suppressed even at high temperature. In addition, since the bonding force between Ni and Si in Ni_ySi_{1-y} (where, $0<y<1$, more preferably $0.4\leqq y\leqq 0.75$) is strong, the first metal contacting with AlGaN electron supplying layer 35 is more stable than simple Ni at high temperature. Especially, in the case of $0.65\leqq y\leqq 0.75$, the melting point is extremely high, approximately at 1200°C or higher. In addition, an increase of the resistivity is small compared with Ni. For this reason, thermal diffusion of the metal of the first metal layer into the AlGaN electron supplying layer 35 is suppressed even at high temperature. As a result, the reliability of the device is improved.

In this embodiment, as with the first and the second embodiments, the improvement of thermal stability of the gate electrode has been confirmed. In addition, the improvement of power performance due to the improvement of thermal resistance of the gate electrode has also been confirmed.

In this embodiment according to the present invention, although the first metal layer (371) was configured with a Ni_ySi_{1-y} layer, the foregoing effect can be obtained even if the first metal layer is replaced with metal silicates or metal nitrides having a large work function and a high thermal stability, for example, PtSi, PdSi, NiN, and PdN. It is more favorable to replace the first metal layer with any one of Pt_ySi_{1-y} (where, $0.5\leqq y\leqq 0.75$), Pd_ySi_{1-y} (where, $0.5\leqq y\leqq 0.85$), Ni_yN_{1-y} (where, $0.5\leqq y\leqq 0.85$), and Pd_yN_{1-y} (where, $0.5\leqq y\leqq 0.85$).

In this embodiment according to the present invention, although the second metal layer was configured with a Mo layer, the foregoing effect can be obtained even if the Mo layer is replaced with other refractory metals. For example, the second metal layer 372 may be replaced with any one of a Pt layer, a W layer, a Ti layer, and a Ta layer. The same effect can also be obtained even if the second metal layer (372) is replaced with metal silicates or metal nitrides having a high melting point and a high thermal stability. For example, the second metal layer (372) may be replaced with any one of a Mo_xSi_{1-x} layer, a Pt_xSi_{1-x} layer, a W_xSi_{1-x} layer, a Ti_xSi_{1-x} layer, a Ta_xSi_{1-x} layer, a Mo_xN_{1-x} layer, a W_xN_{1-x}, a Ti_xN_{1-x} layer, and a Ta_xN_{1-x} layer (where, $0<x<1$).

In this embodiment, the third metal layer was configured with an Au layer 373. However, the same effect can be obtained even if the third metal layer (373) is replaced

with other metal layer having a low resistivity. For example, the third metal layer (373) may be replaced with any one of a Cu layer, an Al layer, and a Pt layer.

(Fourth Embodiment)

Next, a fourth embodiment according to the present invention will be described by referring to Fig. 6.

Fig. 6 is a figure showing a cross sectional structure of a GaN metal-semiconductor field-effect transistor (MESFET) in the fourth embodiment according to the present invention. The MESFET is configured on a semiconductor layer formed on a SiC substrate 41. On the SiC substrate 41, an undoped AlN buffer layer 42 is formed, an undoped GaN buffer layer 43 (film thickness: 1 μm) is formed on the undoped AlN buffer layer 42, and a n-type GaN channel layer 44 (impurity concentration: $2 \times 10^{17}/cm^3$, film thickness: 150 nm) is formed on the undoped GaN buffer layer 43, sequentially.

A source electrode 6S and a drain electrode 6D are formed in contact with an upper surface of the n-type GaN channel layer 44 to form ormic contact.

Next, a gate electrode 47 having a laminated structure comprising a Ni layer 471 as a first metal layer which contact with the GaN channel layer 44, a Mo layer 472 as a second metal layer, and an Au layer 473 as a third metal layer, is formed in Schottky contact. A depletion layer is generated in the n-type GaN channel layer 44 in the vicinity of interface with the gate electrode 47. The MESFET can be operated as a transistor by modulating a width of the depletion layer with a potential of the gate electrode 47. In this embodiment, the channel layer was formed with n-type GaN, however, this may be replaced with n-type InGaN.

This embodiment is a GaN MESFET to which the gate electrode structure 17 shown in Fig. 1 is applied. Therefore, as with the first embodiment, the interdiffusion between the first metal layer and the third metal layer is suppressed even at high temperature. As a result, the improvement of the device reliability can be achieved. In addition, a high Schottky barrier and a good Schottky contact can be obtained. Further, the gate electrode 47 may be replaced with the gate electrode structure 27 shown in Fig. 4. In this case, as with the second embodiment, the thermal diffusion of Ni into the GaN channel layer 44 is suppressed even at high temperature, thereby the device reliability is improved. Furthermore, the gate electrode 47 may be replaced with the gate electrode structure 37 shown in Fig. 5. In this case, as with the third embodiment, the thermal diffusion of the first metal layer into the GaN channel layer 44

is suppressed as well as the interdiffusion between the first metal layer and the third metal layer is suppressed, thereby resulting in the improvement of the device reliability.

(Fifth Embodiment)

Next, a fifth embodiment according to the present invention will be described by referring to Fig. 7.

Fig. 7 is a figure showing a cross sectional structure of a GaN/AlGaN HJFET in the fifth embodiment according to the present invention. The HJFET is configured with semiconductor layers formed on a GaN substrate 51. On the GaN substrate 51, an undoped AlN buffer layer 52 is formed, an undoped AlGaN buffer layer 53 (film thickness: 1 μm) is formed on the undoped AlN buffer layer 52, a n-type AlGaN electron supplying layer 54 composed of $Al_{0.2}Ga_{0.8}N$ (impurity concentration: 2 x $10^{18}/cm^3$, film thickness: 30 nm) is formed on the undoped AlGaN buffer layer 53, and an undoped GaN channel layer 55 is formed on the n-type AlGaN electron supplying layer 54, sequencially, to form a stacked semiconductor layer.

A source electrode 6S and a drain electrode 6D are formed in contact with an upper surface of the GaN channel layer 55 forming an ormic contact. In addition, a gate electrode 57 having a laminate structure comprising a NiSi layer composed of $Ni_{0.5}Si_{0.5}$ as a first metal layer and an Au layer 572 as a second metal layer is formed in contact with an upper surface of the GaN channel layer 55 forming an ormic contact. A two-dimensional electron gas is generated within the GaN channel layer 55 in the vicinity of interface with the AlGaN electron supplying layer 54. The HJFET operates as a transistor by modulating the two-dimensional electron gas concentration with a potential of the gate electrode 57. In this embodiment, although the channel layer was formed with GaN, it may be replaced with InGaN.

In this embodiment, the gate electrode structure 27 shown in Fig. 4 has been applied to a GaN/AlGaN HJFET. Therefore, as with the second embodiment, the thermal diffusion of the first metal layer into the GaN channel layer 55 is suppressed even at high temperature. As a result, the device reliability can be improved.

The gate electrode 57 may be replaced with the gate electrode structure 17 shown in Fig. 1. In this case, as with the first embodiment, the interdiffusion between the first metal layer and the third metal layer is suppressed even at high temperature, thereby the device reliability can be improved. In addition, the Schottky barrier is high, then, a good Schottky contact can be obtained.

Furthermore, the gate electrode 57 may be replaced with the gate electrode structure 37 shown in Fig. 5. In this case, as with the third embodiment, the thermal

diffusion of the first metal layer into GaN channel layer 55 is suppressed as well as the interdiffusion between the first metal layer and the third metal layer is suppressed, thereby resulting in improvement of the device reliability.

Although the present invention has been explained in relation to some of the preferred forms and embodiments, it can be understood that these forms and embodiments serve merely as examples provided to describe the invention, and they are not intended to limit the present invention to these forms and embodiments.

For example, in the above embodiments, a GaN layer or an AlGaN has been used as a semiconductor layer to which a Schottky junction electrode contacts. However, an InAlN layer, an InGaN layer, an InAlGaN layer, and an AlN layer may be used for it. Also, a super lattice layer comprising at least any one of a GaN layer, an AlGaN layer, an InAlN layer, an InGaN layer, an InAlGaN layer, and AlN layer, may be used.

In addition, in the above embodiments, the source electrode, the gate electrode, and the drain electrode had planar structures formed on the same semiconductor layer. However, a recess structure in which a cap layer of n-type semiconductor is selectively formed under the source electrode and the drain electrode may also be used. Furthermore, a buried gate structure buried in a semiconductor layer such as a GaN layer and an AlGaN layer may be used.

[Advantages of the Invention]

According to the present invention described in the above, in GaN semiconductor devices, the Schottky junction electrode is configured with a stacked layer structure comprising the first metal layer formed with any one of Ni, Pt, and Pd, the second metal layer formed with any one of Mo, Pt, W, Ti, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xNi_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, Ta_xN_{1-x} (where, $0<x<1$), and the third metal layer formed with any one of Au, Cu, Al, and Pt. With the above configuration, the interdiffsion between the first metal and the third metal is suppressed, thereby resulting in the reliability improvement. In addition, since a work function of the first metal is large, the Schottky barrier becomes high. As a result, a good Schottky contact can be obtained.

Furthermore, if the Schottky junction electrode is configured with a stacked layer structure comprising the first metal layer formed with any one of Ni_ySi_{1-y}, Pt_ySi_{1-y}, Pd_ySi_{1-y}, Ni_yN_{1-y}, and Pd_yN_{1-y} (where, $0<y<1$) and the second metal layer formed with any one of Au, Cu, Al, and Pt, the thermal diffusion of the first metal into the GaN semiconductor is suppressed, thereby resulting in the reliability improvement.

Accordingly, the present invention contributes to high temperature performance and high output power of the semiconductor device.

[Brief description of the drawings]

Fig. 1 is a figure showing a cross sectional structure of a HJFET in the first embodiment according to the present invention;

Fig. 2 is a diagram showing a gate reverse current – voltage characteristics before and after a heat treatment of the semiconductor device shown in Fig. 1;

Fig. 3 is a diagram showing a gate width dependency of saturated output density of a semiconductor device in this embodiment, compared with that of a conventional semiconductor device;

Fig. 4 is a figure showing a cross sectional structure of a HJFET in the second embodiment according to the present invention;

Fig. 5 is a figure showing a cross sectional structure of a HJFET in the third embodiment according to the present invention;

Fig. 6 is a figure showing a cross sectional structure of a MESFET in the fourth embodiment according to the present invention;

Fig. 7 is a figure showing a cross sectional structure of a HJFET in the fifth embodiment according to the present invention;

Fig. 8 is a cross sectional view of a conventional semiconductor device;

Fig. 9 is a diagram showing a gate reverse current – voltage characteristics before and after a heat treatment of a conventional semiconductor device;

Fig. 10 is a diagram showing Auger profiles of a conventional semiconductor device before a heat treatment;

Fig. 11 is a diagram showing Auger profiles of a conventional semiconductor device after a heat treatment.

[Explanation of symbol]

6D: drain electrode

6S: source electrode

11, 21, 61: sapphire substrate

12, 22, 32, 42, 52, 62: AlN buffer layer

13, 23, 55, 63: GaN channel layer

14, 24, 35, 64: AlGaN electron supplying layer

17, 27, 37, 47, 57, 67: gate electrode

171, 471, 671: Ni layer

172, 372, 472: Mo layer

173, 272, 373, 473, 572, 672: Au layer

271, 371, 571: NiSi layer

31, 41: SiC substrate

33, 43: GaN buffer layer

34: InGaN channel layer

44: n-type GaN channel layer

51: GaN substrate

53: AlGaN buffer layer

54: n-type AlGaN electron supplying layer

FIG. 1

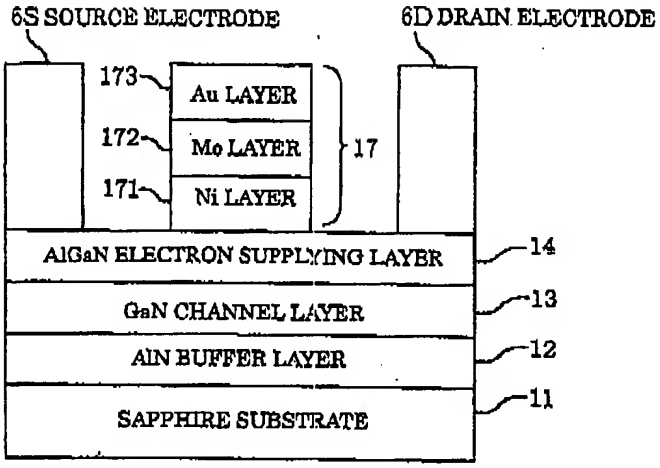


FIG. 2

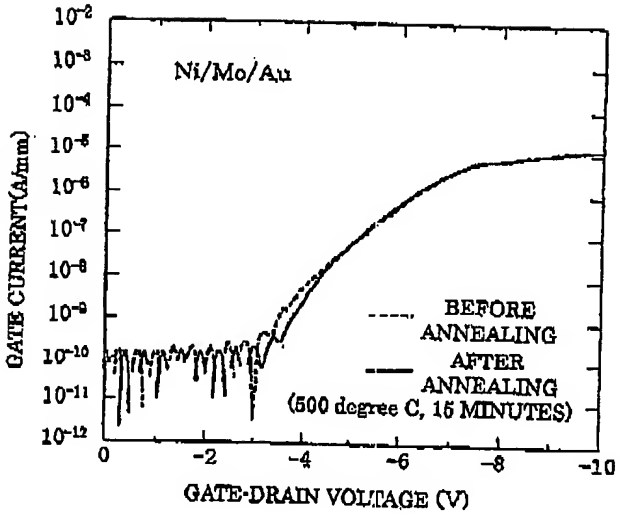

Ni/Mo/Au
BEFORE ANNEALING
AFTER ANNEALING
(500 degree C, 15 MINUTES)
GATE CURRENT(A/mm)
GATE-DRAIN VOLTAGE (V)
0
-2
-4
-6
-8
-10

FIG. 3

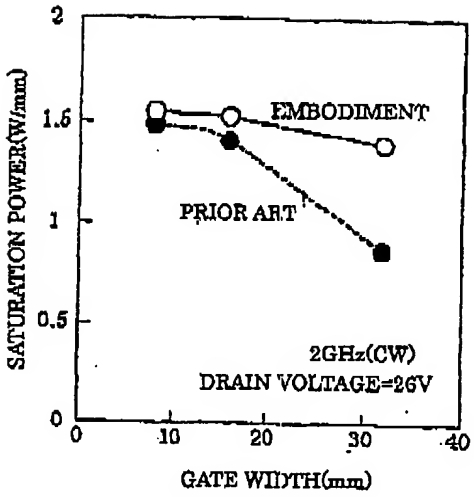

2
1.6
1
0.5
0
SATURATION POWER(W/mm)
EMBODIMENT
PRIOR ART
2GHz(CW)
DRAIN VOLTAGE=26V
0
10
20
30
40
GATE WIDTH(mm)

FIG. 4

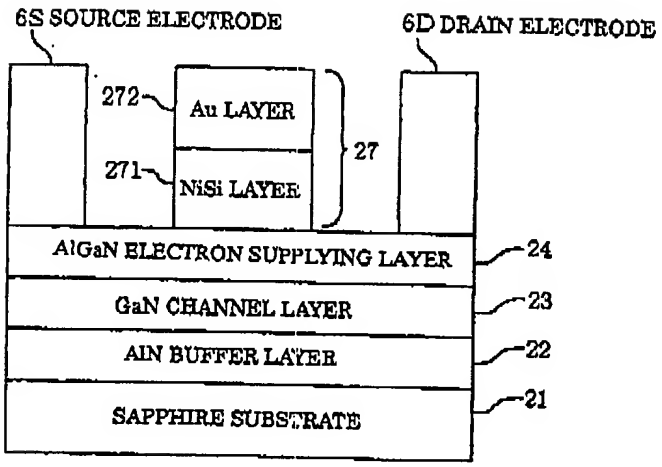

6S SOURCE ELECTRODE
6D DRAIN ELECTRODE
272
Au LAYER
271
NiSi LAYER
27
AlGaN ELECTRON SUPPLYING LAYER
24
GaN CHANNEL LAYER
23
AlN BUFFER LAYER
22
SAPPHIRE SUBSTRATE
21

FIG. 5

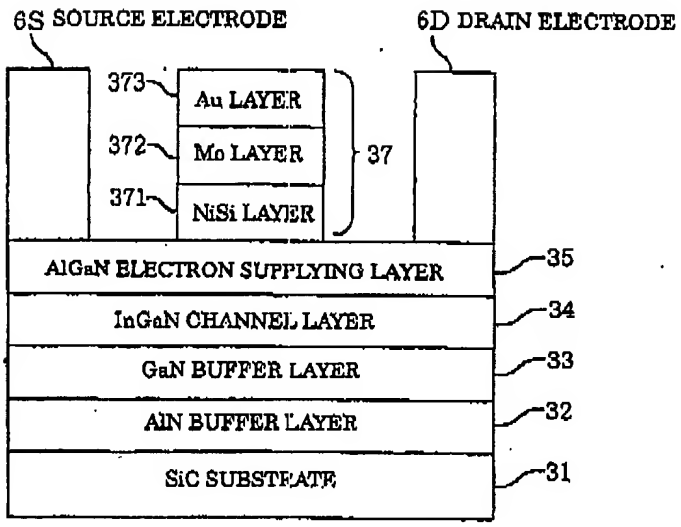

6S SOURCE ELECTRODE
6D DRAIN ELECTRODE
373
Au LAYER
372
Mo LAYER
37
371
NiSi LAYER
AlGaN ELECTRON SUPPLYING LAYER
35
InGaN CHANNEL LAYER
34
GaN BUFFER LAYER
33
AlN BUFFER LAYER
32
SiC SUBSTRATE
31

FIG. 6

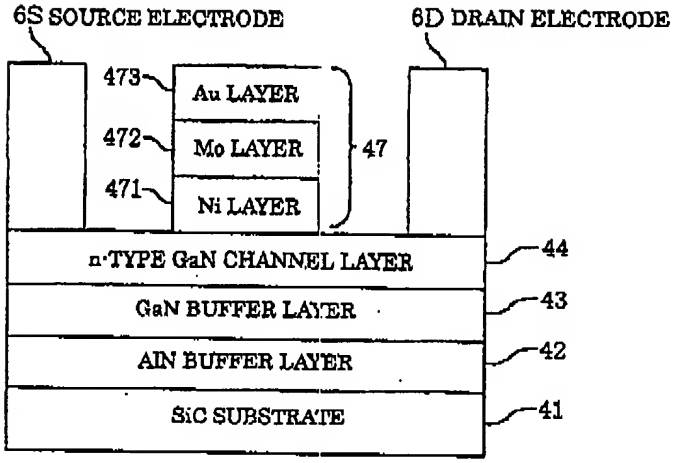

6S SOURCE ELECTRODE
6D DRAIN ELECTRODE
473
Au LAYER
472
Mo LAYER
47
471
Ni LAYER
n-TYPE GaN CHANNEL LAYER
44
GaN BUFFER LAYER
43
AlN BUFFER LAYER
42
SiC SUBSTRATE
41

FIG. 7

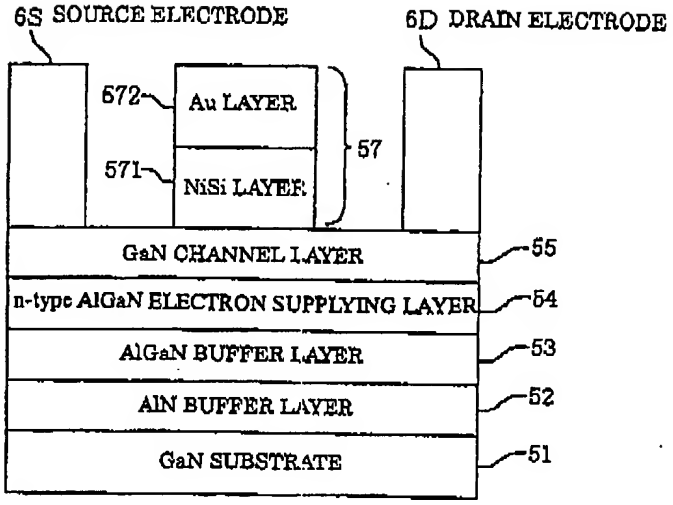

6S SOURCE ELECTRODE
6D DRAIN ELECTRODE
572
Au LAYER
571
NiSi LAYER
57
GaN CHANNEL LAYER
55
n-type AlGaN ELECTRON SUPPLYING LAYER
54
AlGaN BUFFER LAYER
53
AlN BUFFER LAYER
52
GaN SUBSTRATE
51

FIG. 8

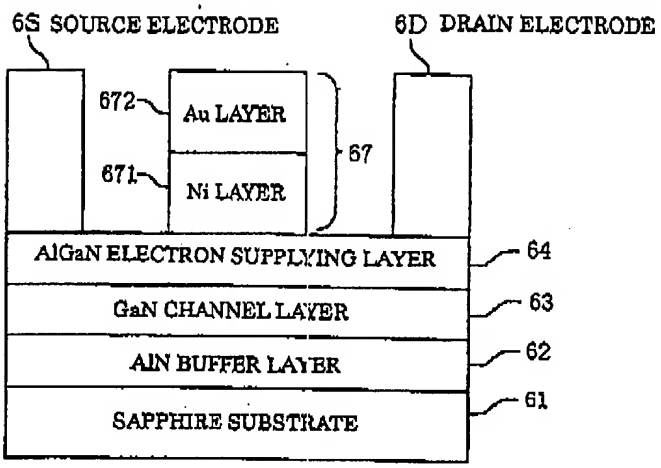

6S SOURCE ELECTRODE
6D DRAIN ELECTRODE
672
Au LAYER
671
Ni LAYER
67
AlGaN ELECTRON SUPPLYING LAYER
64
GaN CHANNEL LAYER
63
AlN BUFFER LAYER
62
SAPPHIRE SUBSTRATE
61

FIG. 9

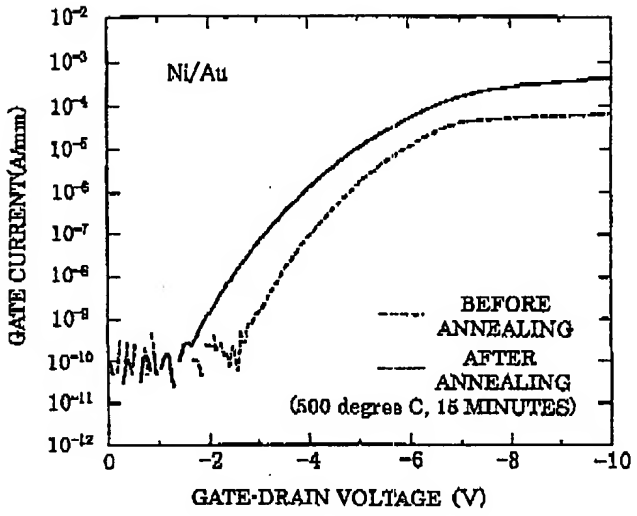

Ni/Au
BEFORE ANNEALING
AFTER ANNEALING
(500 degree C, 15 MINUTES)
GATE CURRENT(A/mm)
GATE-DRAIN VOLTAGE (V)
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
0
-2
-4
-6
-8
-10

FIG. 10

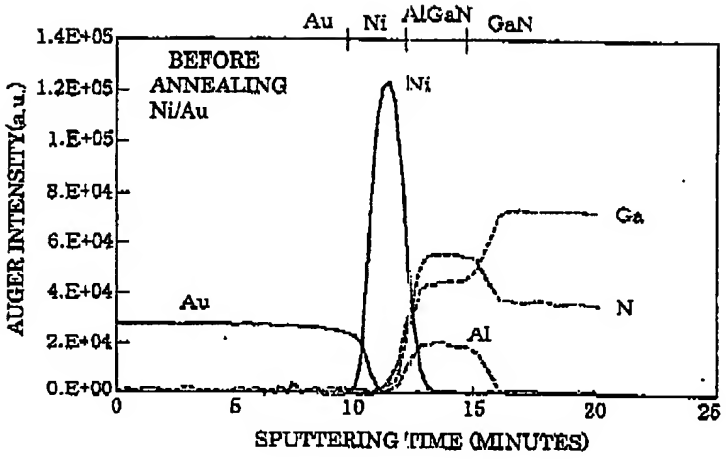
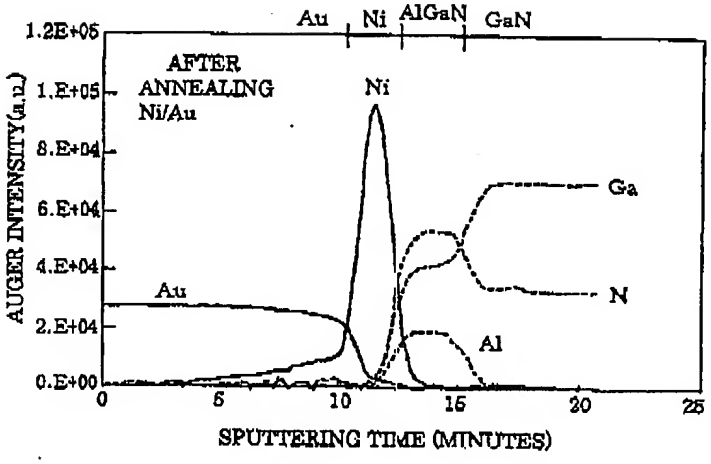

Au
Ni
AlGaN
GaN
BEFORE
ANNEALING
Ni/Au
Ni
Ga
N
Al
Au
AUGER INTENSITY(a.u.)
1.4E+05
1.2E+05
1.E+05
8.E+04
6.E+04
4.E+04
2.E+04
0.E+00
0
5
10
15
20
25
SPUTTERING TIME (MINUTES)

FIG. 11


Au
Ni
AlGaN
GaN
AFTER
ANNEALING
Ni/Au
Ni
Ga
N
Au
Al
AUGER INTENSITY(a.u.)
1.2E+05
1.E+05
8.E+04
6.E+04
4.E+04
2.E+04
0.E+00
0
5
10
15
20
25
SPUTTERING TIME (MINUTES)